FIG.16A

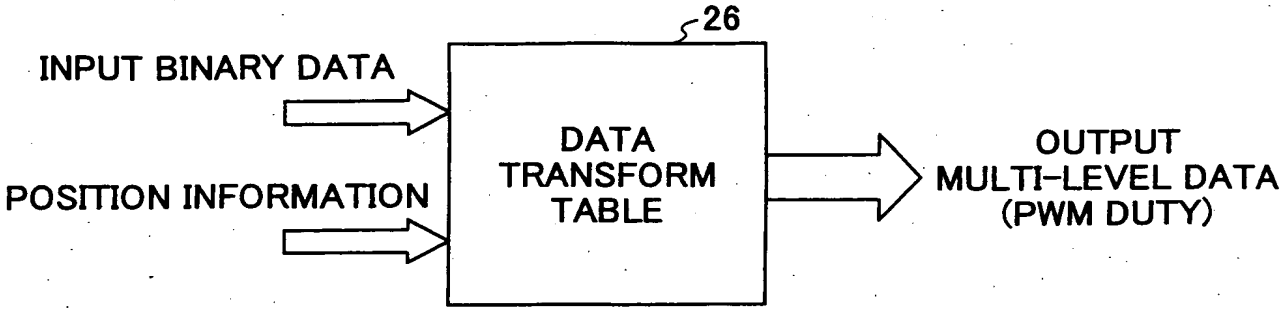

FIG.16B

INPUT BINARY DATA ABCD	POSITION INFORMATION	OUTPUT MULTI-LEVEL DATA (PWM DUTY)	PHASE
≀	≀	≀	≀
1110	a b c d e f g h i	100% 100% 100% 0% 100% 100% 75% 50% 50%	— — — — — — −1 0 −1
≀	≀	≀	≀